MICROCONTROLLER

UNIT–III

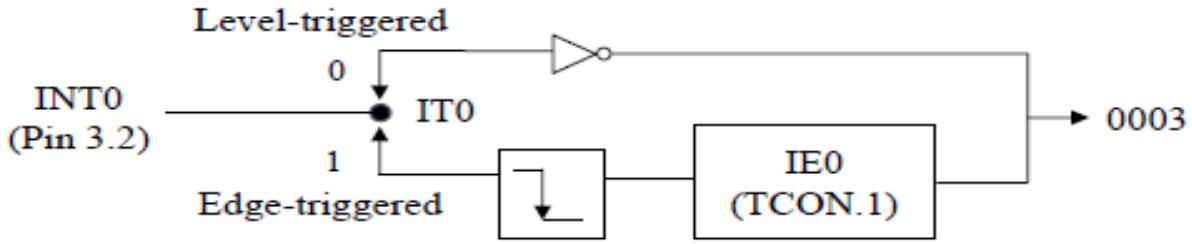
Lecture–7

EXTERNAL HARDWARE INTERRUPTS

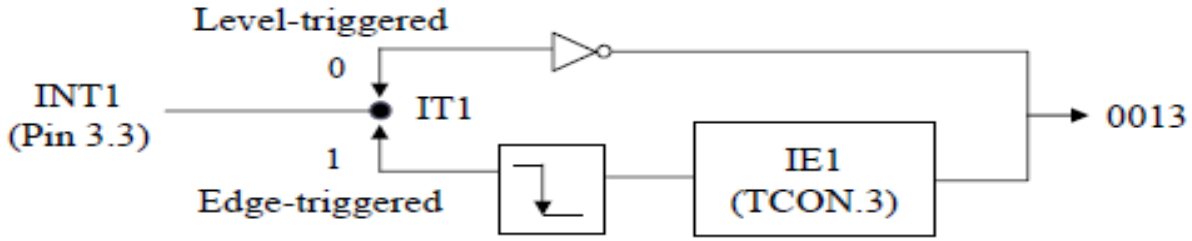
- The 8051 has two external hardware interrupts
- Pin 12 (P3.2) and pin 13 (P3.3) of the 8051, designated as INT0 and INT1, are used as external hardware interrupts
- The interrupt vector table locations 0003H and 0013H are set aside for INT0 and INT1
- There are two activation levels for the external hardware interrupts
- Level trigged and Edge trigged

Contd.

Activation of INT0



Activation of INT1



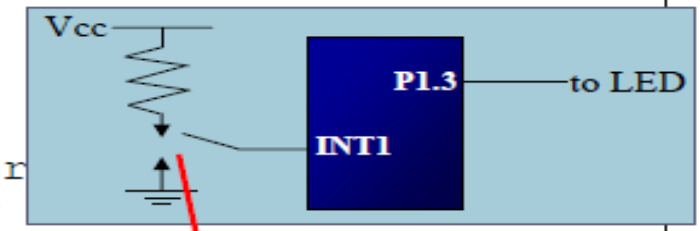
Level-Triggered Interrupt

- In the level-triggered mode, INT0 and INT1 pins are normally high
- If a low-level signal is applied to them, it triggers the interrupt
- Then the microcontroller stops whatever it is doing and jumps to the interrupt vector table to service that interrupt
- Low-level signal at the INT pin must be removed before execution of the last instruction of the ISR, RETI; otherwise, another interrupt will be generated

Contd.

Example 11-5

Assume that the INT1 pin is connected to a switch that is normally high. Whenever it goes low, it should turn on an LED. The LED is connected to P1.3 and is normally off. When it is turned on it should stay on for a fraction of a second. As long as the switch is pressed low, the LED should stay on.



Solution:

```
        ORG   0000H
        LJMP  MAIN ;by-pass inter
                   ;vector table
;--ISR for INT1 to turn on LED
        ORG   0013H      ;INT1 ISR
        SETB  P1.3       ;turn on LED
        MOV   R3,#255
BACK:   DJNZ  R3,BACK    ;keep LED on for a
        CLR   P1.3       ;turn off the LED
        RETI             ;return from ISR

;--MAIN program for initialization
        ORG   30H
MAIN:   MOV   IE,#10000100B ;enable external INT 1
HERE:   SJMP  HERE       ;stay here until get interrupted
        END
```

Pressing the switch will cause the LED to be turned on. If it is kept activated, the LED stays on

Sampling Low Level-Triggered Interrupt

- Pins P3.2 and P3.3 are used for normal I/O unless the INT0 and INT1 bits in the IE register are enabled
- After the hardware interrupts in the IE register are enabled, the controller keeps sampling the INTn pin for a low-level signal once each machine cycle
- According to one manufacturer's data sheet,
- The pin must be held in a low state until the start of the execution of ISR

Contd.

- If the INTn pin is brought back to a logic high before the start of the execution of ISR there will be no interrupt
- If INTn pin is left at a logic low after the RETI instruction of the ISR, another interrupt will be activated after one instruction is executed
- To ensure the activation of the hardware interrupt at the INTn pin, make sure that the duration of the low-level signal is around 4 machine cycles, but no more

Edge-Triggered Interrupt

- To make INT0 and INT1 edge triggered interrupts, we must program the bits of the TCON register
- The TCON register holds, among other bits, the IT0 and IT1 flag bits that determine level- or edge-triggered mode of the hardware interrupt
- IT0 and IT1 are bits D0 and D2 of the TCON register

Contd.

- They are also referred to as TCON.0 and TCON.2 since the TCON register is bit addressable
- This is due to the fact that the level-triggered interrupt is not latched